PTO/SB/21 (09-04) Approved for use through 07/31/2006. OMB 0651-0031 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE ction of information unless it displays a valid OMB control number. erwork Reduction Act of 1995, no persons are required to respond to a co **Application Number** 10/724,996 TRANSMITTAL Filing Date December 01, 2003 First Named Inventor **FORM** Hils, Andreas Art Unit 2825 **Examiner Name** Siek, Vuthe (to be used for all correspondence after initial filing) Attorney Docket Number 03-0352 Total Number of Pages in This Submission **ENCLOSURES** (Check all that apply) After Allowance Communication to TC Fee Transmittal Form Drawing(s) Appeal Communication to Board Licensing-related Papers Fee Attached of Appeals and Interferences Appeal Communication to TC Petition (Appeal Notice, Brief, Reply Brief) Amendment/Reply Petition to Convert to a **Proprietary Information** After Final Provisional Application Power of Attorney, Revocation Status Letter Affidavits/declaration(s) Change of Correspondence Address Other Enclosure(s) (please Identify **Terminal Disclaimer Extension of Time Request** below): Request for Refund **Express Abandonment Request** 1. Copy of Cited References CD, Number of CD(s) Information Disclosure Statement 2. Return Postcard Landscape Table on CD Certified Copy of Priority Remarks Document(s) - IDS Filing Reply to Missing Parts/ Incomplete Application Reply to Missing Parts under 37 CFR 1.52 or 1.53 SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT Firm Name LSI Logic Corporation Signature

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36,771

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Timothy R. Croll

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This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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For	r FY 2	006	L	First Named In	ventor	Hils, A	ndreas	
Applicant claims small	entity status	See 37 CER 1 1	,,,	Examiner Nam	e	Siek, V	uthe/	
				Art Unit		2825		
TOTAL AMOUNT OF PAY	MENT (\$)	180.00		Attorney Docke	et No.	03-035	2	
METHOD OF PAYMENT	「(check all	that apply)						
Check Credit (	Card I	Money Order	None	Other (	please ide	entify):		
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under 37 CFR WARNING: Information on this information and authorization	form may be	come public. Cred	it card info	rmation should r	not be inc	luded on	this form. F	Provide credit card
FEE CALCULATION (A			upon fili	ng or may be	subjec	t to a s	urcharge	e.)
1. BASIC FILING, SEAR	FILING	FEES Small Entity	SEAR	CH FEES Small Entity	_	Sm:	ON FEES	
Application Type	Fee (\$)	Fee (\$)	Fee (\$)	Fee (\$)	Fee		ee (\$)	Fees Paid (\$)
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Design Plant	200 200	100	100	50	130		65	
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2. EXCESS CLAIM FEE		100	U	0	,	J	0	Small Entity
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Each claim over 20 (i Each independent cla			ues)				200	100
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HP = highest number of independent claims paid for, if greater than 3.  3. APPLICATION SIZE FEE								
If the specification and	drawings e							
listings under 37 CFR 1.52(e)), the application size fee due is \$250 (\$125 for small entity) for each additional 50								
sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).  Total Sheets  Extra Sheets  Number of each additional 50 or fraction thereof  100 = /50 = (round up to a whole number) x =								
- 100 = / 50 = (round <b>up</b> to a whole number) x = 4. OTHER FEE(S) Fees Paid (\$)  Non-English Specification, \$130 fee (no small entity discount)								
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SUBMITTED BY			
Signature	12this	Registration No. (Attorney/Agent) 36,771	Telephone (408) 433-7625
Name (Print/Type	e) Timothy R. Croll		Date 72 F&B 66

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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re Application of:

Andreas Hils et. al.

Serial No.:

10/724,996

Filed:

December 01, 2003

For:

Integrated Circuits, and Design and

Manufacture Thereof

10724996

FEB 2 8 2006 W

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date below:

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**Group Art Unit:** 

Examiner:

Atty Docket:

Signature

03/01/2006 HTECKLU1 00000025 122252

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INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents P. O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

The references listed in the attached form, copies of which are attached, may be material to examination of above-identified application. Applicants submit these references in compliance with their duty of disclosure pursuant to 37 CFR 1.56 and 1.97.

It is requested that the information disclosed herein be made of record in the application.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

If it is determined that any additional fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 12-2252.

LSI Logic Corporation 1621 Barber Lane, MS D-106 Milipitas, CA 95035

408-433-7475

Date: UV

Respectfully submitted,

**Timothy Croll** 

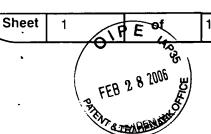
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## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

	Complete if Known				
	Application Number	10/724,996			
	Filing Date	December-01, 2003			
	First Named Inventor	Andreas Hils			
	Group Art Unit	2825			
_	Examiner Name	Vuthe Siek			
	Attorney Docket No.	1496 00327 / 03-0352			



OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, caalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T
		"Submicron CMOS Gate Array", IBM Technical Disclosure Bulletin, Volume 33, No. 3B, August 1990, pages 129-131	
		"An Integrated Design Flow for a Via-Configurable Gate Array", Ran et al., Computer Aided Design, 2004, ICCAD-2004, IEEE/ACM International Conference, November 7-11, 2004, pages 582-589	
		"Structured ASICs: Opportunities and Challenges", Zahiri, Proceedings 2003 IEEE International Conference on Computer Design: VLSI in Computers and Processors, ICCD 2003, October 13-15, 2003, pages 404-409	

Examiner	Date
signature	considered